MULTIPLE SHEETS

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IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 9 with the following:

Referring again to FIG. 2, the interpolator 18 generates the weighting signals $\alpha_1, \alpha_2, \ldots \alpha_N$ in response to the control signal V_{CTRL}. In a preferred embodiment, the weighting signals are a series of continuous, overlapping Gaussian-shaped current pulses having a centroid whose location moves along the length of the interpolator as V_{CTRL} is varied so that most of the weighting signals are nearly zero, but adjacent stages near the centroid are enabled to some extent. Also, the sum of all the weighting coefficients are typically, though not necessarily, a constant value α_{FS}:

$$\sum_{k=1}^{N} \alpha_k = \alpha_{FS} \qquad \text{(Eq. 15)}$$

An interpolator capable of generating Gaussian-shaped current pulses meeting these requirements is disclosed in U.S. Patent No. 5,077,541 by the same inventor as the present application. In a preferred embodiment, the interpolator is of the type described in ~~co-pending~~ U.S. Patent Application Ser. No. 09/466,050, Attorney Docket No. 1482-117, filed December 17, 1999 , which is now U.S. Patent No. 6,489,849, entitled "Interpolator Having Dual Transistor Ranks and Ratiometric Control" by the same inventor as the present application and which is incorporated by reference.

Please replace the paragraph beginning at page 1, line 9 with the following:

FIG. 8 is a schematic diagram of a preferred embodiment of an amplifier cell suitable for use in a practical implementation of the circuit of FIG. 2. The amplifier of FIG. [[7]] 8 is based on the circuits disclosed in U.S. Patent Application Ser. No. 09/241,359 titled "Logarithmic Amplifier With Self-Compensating Gain For Frequency Range Extension" filed January 29, 1999, which is now U.S. Patent No. 6,144,244, by the same inventor as the present application, and which is herein incorporated by reference.